## CLAIM

1. A production method for manufacturing a plurality of chip-size packages, which comprises:

defining a plurality of semiconductor chip areas on a surface of a wafer, with each of said semiconductor chip areas being produced as a semiconductor device having a plurality of electrode pads formed thereon;

forming a plurality of sprout-shaped metal bumps on each of said semiconductor devices such that said respective sprout-shaped metal bumps are bonded on said electrode pads formed on a corresponding semiconductor device;

forming a resin-sealing layer on the surface of said wafer such that tips of said sprout-shaped metal bumps formed on each of said semiconductor devices are projected from a top surface of said resin-sealing layer;

forming a plurality of wiring patterns on the top surface of said resin-sealing layer such that each of said wiring patterns is allocated to a corresponding semiconductor device, and such that electrical connections are established between each of said wiring patterns and the tips of said sprout-shaped metal bumps formed on the corresponding semiconductor device; and

forming a plurality of outer electrode terminals on each of said wiring patterns such that electrical connections are established therebetween, whereby each of said semiconductor devices is produced as a resin-sealed chip-size package on said wafer.

2. A production method as set forth in claim 1, further comprising dicing said wafer such that said resin-sealed chip-size packages are individually separated therefrom.

3. A production method as set forth in claim 1, wherein each of said wiring patterns includes a plurality of

conducting paths, and each of said outer electrode terminals is configured as a metal ball, with the metal ball being soldered and bonded on one of said conducting paths.

4. A production method as set forth in claim 3, wherein a solder resist layer is formed on the top surface of said resin-sealing layer after the forming of said metal balls, and is patterned such that a plurality of openings are formed to solder and bond said respective metal balls to said conducting paths though the openings formed in said solder resist layer.

5. A production method as set forth in claim 1, wherein, in the forming of said sprout-shaped metal bumps, each of said sprout-shaped metal bumps is produced from a metal wire, using a wire-bonding machine, and each of said sprout-shaped metal bumps has a base portion bonded on a corresponding electrode pad, and a cone-like portion integrally protruded from said base portion.

6. A production method as set forth in claim 5, wherein the production of each of said sprout-shaped metal bumps is carried out by stacking up at least two metal bumps, obtained from said metal wire, using said wire-bonding machine.

7. A production method as set forth in claim 1, wherein the forming of said resin-sealing layer comprises:

preparing an adhesive resin sheet including a film-like support element carrying said sealing-resin layer formed thereon;

laminating said adhesive resin sheet on said wafer such that said sprout-shaped metal bumps are penetrated into the resin-sealing layer of said adhesive resin sheet; and

removing said film-like support element from said adhesive resin sheet, with a thickness of said resin-sealing layer being smaller than an entire height of said sprout-shaped metal bumps, resulting in the projection of the tips of said sprout-shaped metal bumps from the top surface

of said resin-sealing layer.

8. A production method as set forth in claim 7, wherein the forming of said wiring patterns comprises:

forming of a thin metal film on the top surface of said resin-sealing layer;

patterning said thin metal film such that a plurality of film-like metal patterns corresponding to said wiring patterns are formed therein; and

thickening said thin metal film patterns such that said film-like metal patterns grow into said wiring patterns.

9. A production method as set forth in claim 8, wherein the forming of said thin metal film is carried out by using a thin metal film formation process selected from the group consisting of a sputtering process, an electroless plating process, and a vacuum metal deposition process, and the thickening of said thin metal film patterns is carried out by using an electroplating process.

10. A production method as set forth in claim 1, wherein the forming of said resin-sealing layer comprises:

preparing an adhesive resin sheet including a film-like metal support element carrying said sealing-resin layer formed thereon; and

laminating said adhesive resin sheet on said wafer such that said sprout-shaped metal bumps are penetrated into the resin-sealing layer of said adhesive resin sheet, with a thickness of said resin-sealing layer being smaller than an entire height of said sprout-shaped metal bumps, resulting in the projection of the tips of said sprout-shaped metal bumps from the top surface of said resin-sealing layer, whereby the tips of said sprout-shaped metal bumps are in electrical contact with said film-like metal support element.

11. A production method as set forth in claim 10, wherein the forming of said wiring patterns comprises:

patterning said film-like metal support element such that a plurality of film-like metal patterns corresponding to said wiring patterns are formed therein; and

thickening said film-like metal patterns such that said film-like metal patterns grow into said wiring patterns.

12. A production method as set forth in claim 11, wherein the thickening of said thin metal film patterns is carried out by using an electroplating process.

13. A production method as set forth in claim 1, wherein said resin-sealing layer has a thickness of at least 50 μm.

14. A production method for manufacturing a plurality of chip-size packages, which comprises:

defining a plurality of semiconductor chip areas on a surface of a wafer, with each of said semiconductor chip areas being produced as a semiconductor device having a plurality of electrode pads formed thereon;

forming a first wiring-arrangement on the surface of said wafer,

said first wiring-arrangement including

a plurality of first sprout-shaped metal bumps formed on each of said semiconductor devices, such that said respective sprout-shaped metal bumps are bonded on said electrode pads formed on a corresponding semiconductor device,

a first resin-sealing layer formed on the surface of said wafer such that tips of said sprout-shaped metal bumps formed on each of said semiconductor devices are projected from a top surface of said resin-sealing layer, and

a plurality of first wiring patterns formed on the top surface of said first resin-sealing layer such that each of said first wiring patterns is allocated to a corresponding semiconductor device, and such that electrical connections are established between each of said first wiring patterns and

the tips of said first sprout-shaped metal bumps formed on the corresponding semiconductor device;

forming a second wiring-arrangement on said first wiring-arrangement,

said second wiring-arrangement including

a plurality of second sprout-shaped metal bumps formed on and bonded on each of said first wiring patterns so as to be allocated to a corresponding semiconductor device,

a second resin-sealing layer formed on the first wiring patterns formed on said first wiring-arrangement, such that tips of said second sprout-shaped metal bumps are projected from a top surface of said second resin-sealing layer, and

a plurality of second wiring patterns formed on the top surface of said second resin-sealing layer such that each of said second wiring patterns is allocated to a corresponding semiconductor device, and such that electrical connections are established between each of said wiring patterns and the tips of said sprout-shaped metal bumps allocated to the corresponding semiconductor device;

forming a plurality of outer electrode terminals on each of said second wiring patterns such that electrical connections are established therebetween, whereby each of said semiconductor devices is produced as a resin-sealed chip-size package on said wafer.

15. A production method as set forth in claim 14, further comprising dicing said wafer such that said resin-sealed chip-size packages are individually separated therefrom.

16. A production method for manufacturing a plurality of chip-size packages, which comprises:

defining a plurality of semiconductor chip areas on a surface of a wafer, with each of said semiconductor chip areas being produced as a semiconductor device having a

plurality of electrode pads formed thereon;

forming a multi-layered wiring-arrangement on the surface of said wafer, said multi-layered wiring-arrangement including a lowermost wiring-arrangement section securely mounted on the surface of said wafer, an uppermost wiring-arrangement section, and at least one intermediate wiring-arrangement section intervening therebetween,

each of said wiring-arrangement sections including

a resin-sealing layer,

a plurality of wiring patterns formed on a top surface of said resin-sealing layer and allocated to each of said semiconductor devices, and

a plurality of sprout-shaped metal bumps allocated to each of said semiconductor devices and penetrated into said resin-sealing layer such that tips of said sprout-shaped metal bumps are projected from the top surface of said resin-sealing layer,

the plurality of sprout-shaped bumps of said lowermost wiring-arrangement section establish electrical connections between the electrode pads formed on each of said semiconductor devices and the corresponding wiring pattern of said lowermost wiring-arrangement section,

the plurality of sprout-shaped bumps of each of the remaining wiring-arrangement sections except for said lowermost wiring-arrangement section establish electrical connections between the corresponding wiring pattern of the directly-under wiring-arrangement section and the corresponding wiring pattern of said wiring-arrangement section concerned; and

forming a plurality of outer electrode terminals on each of the wiring patterns formed on said uppermost wiring-arrangement such that electrical connections are established therebetween, whereby each of said semiconductor

devices is produced as a resin-sealed chip-size package on said wafer.

17. A production method as set forth in claim 16, further comprising dicing said wafer such that said resin-sealed chip-size packages are individually separated therefrom.